Efficiency Improvement for a DC-DC Quadratic Power Boost Converter by Applying a Switch Turn-off Lossless Snubber Structure Based on Zero Voltage Switching

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***Abstract*—So as to keep the converter in small size, high switching frequencies are normally used. As a result, in higher frequencies, switching losses seriously affect the efficiency. Current and voltage stresses on power switch can be serious problems particularly in high amount of powers where MOSFET switches are generally applied. A snubber circuit can reduce or eliminate spike voltage and currents, decrease the di/dt or dv/dt values on power switch and transfer the power losses on switch to load and increases the lifelong of the switch. This study presents a method for improving the power transmission efficiency for DC-DC Cascaded Boost Converter and uses a passive snubber sub-circuit, which consists of an inductor, a capacitor, and two diodes for reducing the switching loss. The role of resonant capacitor of this structure is discharging directly through the load and is parallel with the power switch. Thus, it is effective in lossless switching and increasing the DC voltage gain of the boost converter. Soft switching is achieved through the use of a LC resonant tank circuit. The tank circuit is responsible for zero voltage switching (ZVS) and zero current switching (ZCS), eliminating the power loss in the switches appreciably. The proposed structure, done by MATLAB SIMULINK based on simulations, has shown more efficiency toward the same structure without snubber circuit. Besides, an application has been conducted in laboratory scales, and results confirm theoretical findings.**

***Index Terms*—Efficiency optimization; Passive snubber circuit; Switching losses; Cascaded DC DC boost converters; Zero voltage switching (ZVS).**

I. INTRODUCTION

Today power converters are presented in many commercial, medical and industrial applications. A majority of these are high power and high current applications.

DC-DC Boost Converters are increasingly employed as front end converters for recent renewable energy sources such as battery sources, photovoltaic (PV) systems and fuel cells (FC). In general, when we need to step up a DC voltage, a boost converter is usually chosen. In recent years, the switching frequency has been increased to minimize the converter size and volume. Unfortunately, increasing the switching frequency leads to switching losses and electromagnetic interference (EMI) problem. In order to overcome these problems, soft switching methods are widely used. Soft switching techniques include Zero Current (ZCS) and Zero Voltage (ZVS) switching. In the ZCS and ZVS techniques where the switches are turned on or off at zero current or zero voltage, reducing switching losses will increase the system efficiency [1]–[7]. Without the snubber, ringing can occur. This can happen during the dead time between one transistor turning off and on [8], [9]. During this period, the output loop is closed only by the parasitic series inductances and the parallel capacitors of the MOSFETs. In theory, the subsequent ringing could be twice as high as the input voltage. Poor PCB layout can also be a strong contributor to ringing. The ringing causes electromagnetic interference (EMI) and system noise interference and may exceed the power train transistors' breakdown ratings, resulting in catastrophic circuit failure. The snubber network reduces the ringing down to safe values, at the cost of power dissipated in the resistor. So using snubber circuits have several benefits such as eliminating spike voltage and currents, decreasing the di/d tor dv/dt values and switching losses on power switch and increasing the lifelong of the switch as a result and decreasing the Electromagnetic Interfaces EMI. In literature, different snubber models are investigated. A resistor-capacitor-diode (RCD) snubber for voltage stress reducing on power switch is utilized in [10] but because of resistor in

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this structure exhibits some losses.

An active clamp buck-boost structure was proposed to gain higher efficiency for structure presented in [11]. These structures require an additional power switch and complex control circuits [10]–[14], [8]. Ref. [15] has presented to enhance voltage gain simply by cascade connections of boost converters but the value of output voltage is insufficient for high step-up applications. Resonance converters are a group of soft switching transducers. These converters have high frequency performance, low switching losses, and high efficiency. There are many ways to increase the efficiency of boost converters. For this purpose, some researchers have argued to limit the switching losses and some others have discussed on the limitation of conductive losses. Besides, isolated converters for high operation duty cycles have been designed but these kinds of converters generally have high switch voltage stress on MOSFETs. No isolation is required in cascaded boost converters. The methods to design the conventional types of cascaded boost converters use two or three or several series blocks of conventional boost converters to increase the output voltage. Although increasing the number of boost converters in cascade types can decrease the current stresses in lower stages and voltage stresses in higher stages, it has more losses due to more elements of the circuit [1], [9], [16]. This paper presents a new approach to cascaded boost converters and this is the simulation in MATLAB/SIMULINK by considering resistive and inductance loads. This design has all the advantages of a cascaded boost converter such as reducing voltage and current stress on the converter and the high voltage gain and input current control. In order to prepare the converter structure and inductors in small size, high switching frequencies are generally used. As a result, in higher frequencies switching losses seriously affect the efficiency. Current and voltage stresses on power switch can be serious problems particularly at high power levels where MOSFET switches are generally applied. Nevertheless, there should be a sufficient decrease in the switching losses to maintain a high level of efficiency and enhance the reliability of the power switches. There should be a limitation of the dv/dt of the power switch to reduce the switching losses at high levels current with IGBT or MOSFET. Therefore, a relatively large snubber capacitor must be used in parallel with the switch. The energy stored in this capacitor is proportional to the square of the maximum capacitor voltage. In the case of a boost converter, the value of this voltage is high [17].

Moreover, the energy that is stored in the snubber capacitor must be removed prior to the next turn-off transition and the associated power is proportional to the switching frequency [2]–[7]. Passive snubber circuits are generally simpler to design and have fewer components; therefore, they are less expensive, more reliable, and smaller [2]–[7].

Figure 1 presents conventional cascade DC-DC boost converter which has two power switches. This structure has a simple serial connection between normal boost converters. As it can be seen, it contains two normal boost structures. In this section, a high-efficiency DC-DC boost converter is suggested. It has been shown in Fig. 2. This structure uses only one power switch. In our proposed structure, two-stage cascade boost converter is obtained by adding a (L_2 - D_2 - D_3 - C_2) block to a normal boost converter [1], [18]. When the switch is ON, the current flow from L_2 is charged by V_1 for dT and when it is in OFF mode, the current discharges with – (V_o -V_1) for (1-d)T. The voltage across C_1 charges to V_1 and this value for C2 is Vo.

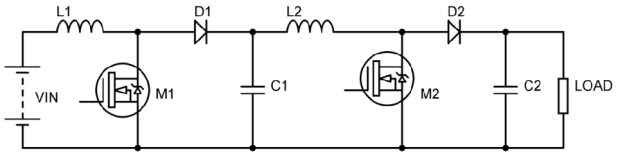


Fig. 1. Conventional cascade DC DC Boost converter.

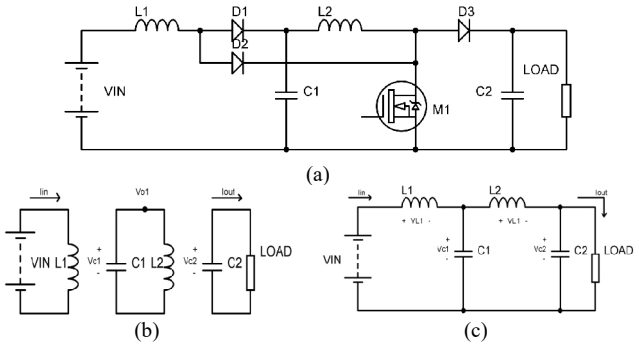


Fig. 2. Cascade DC DC Boost Converter with one power switch (a), circuit when switch is ON (b), circuit when switch is OFF (c).

Then current ripple on L_2 is calculated from

$$\Delta iL_2 = \frac{V_1}{L_2} dT = \frac{Vo - V1}{L_2}(1-d)T. \quad (1)$$

Output voltage and voltage gains are

$$V_o = \frac{1}{1-d} V_1 = (\frac{1}{1-d})^2 V_{in} \rightarrow G = \frac{Vo}{V_{in}} = (\frac{1}{1-d})^2. \quad (2)$$

The currents flow from L_1 and L_2 and current variation on L_1 and L_2 are consequently:

$$\left\{ \begin{array}{ll} \Delta i_{L1} = \frac{Vin}{L_1} dT & I_{L1} = \frac{I_o}{(1-d)^2} \\ \Delta i_{L2} = \frac{V1}{L_2} dT & I_{L2} = \frac{Io}{(1-d)} \end{array} \right\} \rightarrow$$

$$\rightarrow \left\{ \begin{array}{l} \xi_1 = \frac{\Delta i_{L1}/2}{I_{L1}} = \frac{d(1-d)^2 TV_{in}}{2L_1 I_o} = \frac{d(1-d)^4}{2} \frac{R}{fL_1} \\ \xi_2 = \frac{\Delta i_{L2}/2}{I_{L2}} = \frac{d(1-d)TV_1}{2L_2 I_o} = \frac{d(1-d)^2}{2} \frac{R}{fL_2} \end{array} \right\}. \quad (3)$$

Variation ratio of Output voltage on C_2 is

$$\varepsilon = \frac{\Delta vo/2}{Vo} = \frac{1-d}{2RfC_2}. \quad (4)$$

II. SWITCHING LOSSES FOR PROPOSED POWER CONVERTER

One of the most important parameters of power electronic circuits is their efficiency especially when the converter

wants to transfer the generated power by renewable energy resources which produce limited values of power. Efficiency can be computed by comparing the circuit output power to the power delivered by the supply using the following equation

$$\eta = \frac{P_o}{P_{in}} = \frac{V_o I_o}{V_{in} I_{in}} = G(1-D)^2. \quad (5)$$

Equation (5) calculates the overall efficiency of the system and works in practice. Theoretically, a clearer and more precise formula can be written taking into account all the sources of losses

$$\eta = \frac{P_o}{P_{in}} = \frac{P_o}{P_o + P_{loss}}. \quad (6)$$

Particularly in low power sources such as Photovoltaic (PV) or Fuel Cells (FC) and other renewable energy sources it is essential to rise the efficiency of the converter as much as possible to transmit the input power to load. Power losses of the converter can be divided to: conductive, dynamic and fixed losses. The total power loss, P_{loss}, is given with the relation

$$P_{loss} = P_{cond} + P_{fixed} + W_{TOT} \times f_{sw}, \quad (7)$$

where P_{cond} is total conductive losses which are directly dependent on the load current and slightly dependent on the switching frequency f_{sw}. Pfixed is total fixed losses that are independent of the switching frequency and load. W_{TOT} is the total amount of the energy arisen by dynamic losses during one period (Wtransistor, Wdiode, Wcore). Term $W_{TOT} f_{sw}$ in (7), demonstrates overall dynamics losses and is proportional to the switching frequency f_{sw}. All kinds of switching losses for both conventional and quadratic types of converters have been illustrated in Table I. Because of the one power switch existence in proposed structure, it has less value of losses.

TABLE I. SWITCHING LOSSES OF PROPOSED STRUCTURE.

Name of elements	Proposed cascade
MOSFET	$P_{swM} = (w_{on} + w_{off}) f_s$ $w_{off1} = 0.5 i_{L1} V_{c1} T_{off1}$ $w_{on1} = 0.5 i_{L1} V_{c1} T_{on1}$
First Diode	$P_{swD1} = V_{c1} Q_{rr1} f_s$
Second Diode	$P_{swD2} = V_{c2} Q_{rr2} f_s$
Third diode	$P_{swD3} = V_{c3} Q_{rr3} f_s$

In the Table shown above, Q_{rr1}, Q_{rr2} and Q_{rr3} are electrical charges on forward capacitor of D_1, D_2 and D_3. Besides, T_{on1}, T_{on2}, T_{off1} and T_{off2} are times while the switch 1 and switch 2 are short circuited and open circuit consequently.

III. METHODOLOGY

Figure 3 illustrates a MOSFET and C_{GS} is the Gate-Source connection internal capacitor. While the switch is off, sudden increasement in gate voltage by a high dv/dt will drive gate pin of MOSFET by C_{GS}. If this value is high enough, it can turn the switch on. It means that the switch will be on in an undesired time and without applying any control signal. Therefore, it can increase dynamic and frequency losses in a converter structure. The main idea is to apply a parallel capacitor with switch. By this way, with undesired voltage increases in Gate, Drain voltage will increase by an exponential wave form, and it will decrease the possibility of the switch activation. Moreover, with an undesired increase in switch or load current because of a time lackage, it will pass from a narrow place that is for drive circuit in gate pin of switch, causing local heating in Gate pin and harming the switch. Thus, for this purpose we thought to enter an inductor in serial connection with switch. By applying the inductor, the current will increase by an exponential wave form with a small value of di/dt.

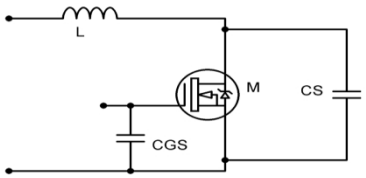


Fig. 3. Snubber sub-circuit structure.

Switching losses and stresses found as a result can pose important problems related to the design, particularly at high power levels where MOSFET or IGBT switches are generally used. In this paper, the aforementioned problem is solved through the judicious use of a lossless snubber subcircuit. It is comprised of a L-C resonant circuit and two diodes. The resonant capacitor of this LC circuit is parallel with the switch and discharges directly through the load, thus maintaining lossless switching and rising the input-output dc gain of the converter. Cascaded Boost converter diagram with proposed passive ZVS is shown in Fig. 4. The snubber circuit, as illustrated, consists of the resonant inductance LS and capacitor CS, the resetting diode D_{S1}, and finally the snubber diode D_{S2}.

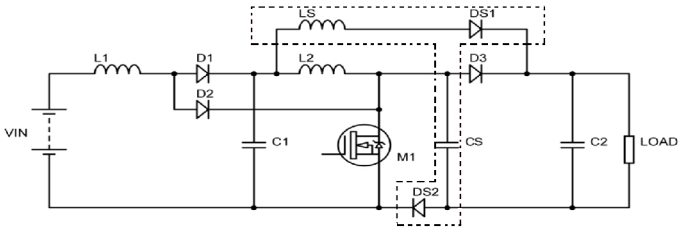


Fig. 4. Snubber circuit added to cascaded boost converter.

Steady state current and voltage waveforms of the MOSFET power switch and inductors for proposed structure are shown in Fig. 5.

It is assumed that the L_2 and C_2 elements are large enough to simplify the calculation analysis. Under these conditions, C_2 and R_{LOAD} voltage may be considered as constant voltage source V_O. Moreover, L_S and C_S are calculated without loss, and M output capacitance and ON-state resistance can be kept small. Assuming that all elements in the circuit are ideal, system has five analysis states during a switching cycle. These situations are given in Fig. 4 and the events in each case are explained under the state. At the beginning, the

M_1 switch is in OFF mode and the diodes D_3 and D_{S2} conduct. Thus, the capacitors C_S and C_2 are connected in parallel to a voltage which is the same as the output voltage V_o.

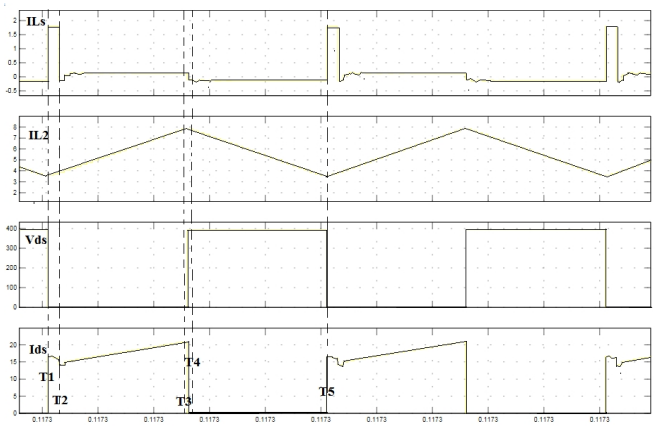


Fig. 5. Steady state current and voltage waveforms of inductors and MOSFET power switch.

Steady state analysis of circuit has presented in five steps by complete equations and figures.

Situation 1: At $t = 0$, switch M_1 is turned on, diode Ds_1 is on and diodes Ds_2 and D_3 are off. As a result, the Cs and C_2 capacitors will be connected in series with L_s inductor. Through the load, the oscillation discharges the capacitor Cs while the boost inductance L_2 stores some energy by means of the switch M_1. Figure 6 shows this state.

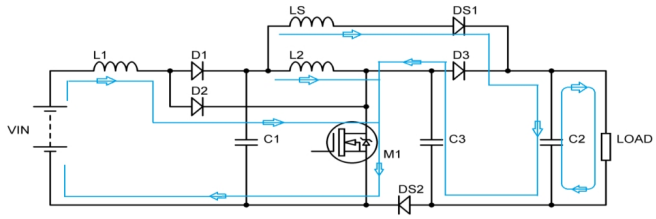


Fig. 6. First state of circuit in a switching cycle.

For $0 < t < T1$, by considering Z_r and W_r, we can calculate voltage and current waveforms of C_s as below:

$$\left.\begin{aligned} Z_r &= \sqrt{\frac{L_s}{C_s}} \\ \omega_r &= \frac{1}{\sqrt{L_s C_s}} \end{aligned}\right\} \rightarrow$$

$$\rightarrow \left\{\begin{aligned} -V_{cs}(t) &= V_i(1-\cos(\omega_r t)) - V_o \\ -i_{cs}(t) &= \frac{Vi}{Zr}\sin(\omega_r t) \end{aligned}\right\}. \qquad (8)$$

So, for t = T1 as boundary condition we will have:

$$\left\{\begin{aligned} -i_{cs}(T1) &= i_{L3}(T1) = \frac{V_i}{Zr}\sin(\omega_r T1) \\ \cos(\omega_r T1) &= 1 - \frac{V_o}{V_i} \end{aligned}\right\}. \qquad (9)$$

Situation 2: At time T = T1, the diode Ds_2 begins to conduct and clamps the voltage on the capacitor Cs. Due to this reason, the fluctuation stops. The L_3 inductance is over-energized, discharged via load and C_2. In other words, the energy is stored in the L_2 inductance via the M_1 switch. This is shown in Fig. 7.

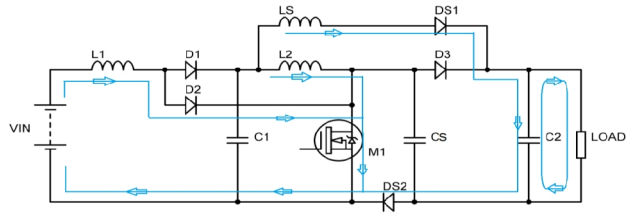


Fig. 7. Second state of circuit in a switching cycle.

So we can find related equation for T1 < t < T2 as below

$$i_{L1}(t) = \frac{V_i - V_o}{L_1}(t - T1) + i_{L3}(T1). \qquad (10)$$

Situation 3: At T = T2, the current in L_3 drops to zero and the Ds1 and Ds2 diodes go into off mode. The current in L_1 linearly stores energy from the input source as a typical boost converter. Figure 8 shows the mode of this cycle. At t = T2 we can see below equation

$$T2 - T1 = \frac{i_L(T1)}{V_o - V_i}. \qquad (11)$$

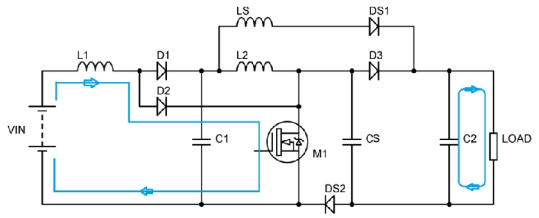


Fig. 8. Third state of circuit in a switching cycle.

For T2 <t <T3

$$i_{L2}(t) = \frac{V_i}{L_2}t + i_{Ls}(0). \qquad (12)$$

Situation 4: At T = T3, the M_1 switch is in the off mode and the Ds_2 diode is in the on-mode. Thus, the current through L_2 is circulating through the capacitor Cs and diode Ds_2. The voltage on capacitor C_1 rises linearly from zero and provides zero voltage transition during shutdown. This is shown in Fig. 9. As mentioned above, M_1 will be turn off at $t = t_{on} = T3$, so as boundary equation of this state we can gain

$$i_{L2}(T3) = \frac{V_i}{L_2}(T3) + i_{L2}(0). \qquad (13)$$

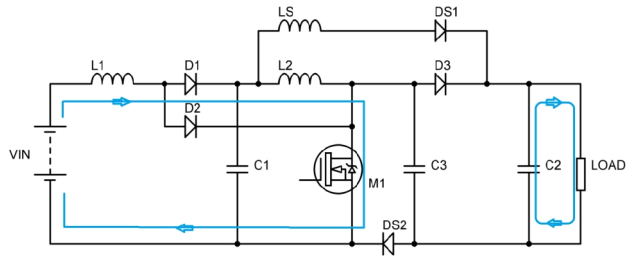


Fig. 9. Fourth state of circuit in a switching cycle.

For T3 <t < T4

$$\left\{\begin{matrix} V_{cs}(t)=\dfrac{i_{L2}(T3)}{C_s}(t-T3) \\ i_{cs}(t)=i_{L2}(T3) \end{matrix}\right\}. \quad (14)$$

Situation 5: At T = T4, diode D_3 goes into conduction mode and the voltage on capacitor Cs reaches output voltage Vo. Energy stored on the L_2 inductance is then released until the M_1 switch is re-opened. This process is repeated from situation 1 after this moment. The final situation is shown in Fig. 10. At T = T4:

$$\left\{\begin{matrix} V_{cs}(T4)=V_o \\ i_{cs}(T4)=0 \end{matrix}\right\} \Rightarrow \left\{\begin{matrix} T4-T3=\dfrac{V_oC_s}{i_{L2}(T3)} \\ i_{L2}(T4)=i_{L2}(T3) \end{matrix}\right\}. \quad (15)$$

For T4 < t < T5 we can illustrate

$$i_{L2}(t)=\frac{V_i-V_o}{L_2}(t-T4)+i_{L2}(T4), \quad (16)$$

so boundary equation will be:

$$\left\{\begin{matrix} i_{L2}(T5)=\dfrac{V_i-V_o}{L_2}(t-T4)+i_{L2}(T4) \\ i_{L2}(T5)=i_{L2}(0) \end{matrix}\right\}. \quad (17)$$

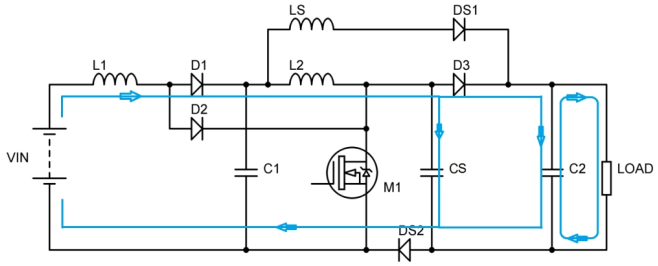


Fig. 10. Fifth state of circuit in a switching cycle.

IV. Discussion on Parameters Values and Simulation Analysis

A. Input Voltage and Load

According to (2), by considering 0.5 for duty cycle, with $V_{in}=100\,VDC$ we will have 400 VDC as output:

$$V_o=\frac{1}{1-d}V_1=(\frac{1}{1-d})^2V_{in}=$$
$$=(\frac{1}{1-0.5})^2\times 100=400\,VDC, \quad (18)$$

$$R_{LOAD}=\frac{V_o{}^2}{P_o}=\frac{400^2}{2000}=80\,\Omega. \quad (19)$$

The maximum output current can be calculated from

$$I_o=\frac{V_o}{R_{Load}}=\frac{400}{80}=5A. \quad (20)$$

B. B. Snubber Circuit Design

The snubber capacitor Cs is calculated as shown in formula 11 with respect to the maximum dv/dt. The maximum current of the PWM amplifier converter at t-T3 is calculated to be equal to 1.3 × I_{lmax}

$$C_s=(1.3)\times(I_{l\max})\times(\frac{dv}{dt})=$$
$$=1.3\times 5\times 41\frac{V}{ns}=266.5\,nF. \quad (21)$$

With a Z value close to 0.20 pu (per unit), the dc gain of the proposed converter is increased by 14 % with the DRC snubber circuit compared to the conventional boost converter. Using this value of Z, the characteristic impedance Zr of the resonant snubber is

$$Z_r=z\times R_{Load}=0.2\times 80=16\,\Omega. \quad (22)$$

Hence, the peak current of the resonant snubber circuit is

$$I_{l\max}=\frac{V_{in}}{Z_r}=\frac{100}{16}=6.25A. \quad (23)$$

Hence

$$Z_r=\sqrt{\frac{L_s}{C_s}}\Rightarrow L_s=C_s\times Z_r{}^2=$$
$$=266.5\,nF\times(16)^2=68.225\,\mu H. \quad (24)$$

C. Calculation of Quadratic Boost Converter Parameters

Refer to (3), with 5 % and 10 % variation for input and second inductors currents and 100 KHz for frequency:

$$\left\{\begin{matrix} \xi_1=\dfrac{\Delta i_{L1}/2}{I_{L1}}=\dfrac{d(1-d)^2TV_{in}}{2L_1I_o}=\dfrac{d(1-d)^4}{2}\dfrac{R}{fL_1} \\ L_1=\dfrac{d(1-d)^4}{2}\dfrac{R}{f\xi_1}=\dfrac{0.5(0.5)^4\times 80}{100K\times 0.05}=500\mu H \end{matrix}\right\}, \quad (25)$$

$$\left\{\begin{matrix} \xi_2=\dfrac{\Delta i_{L2}/2}{I_{L2}}=\dfrac{d(1-d)TV_1}{2L_2I_o}=\dfrac{d(1-d)^2}{2}\dfrac{R}{fL_2} \\ L_2=\dfrac{d(1-d)^2}{2}\dfrac{R}{f\xi_2}=\dfrac{0.5(0.5)^2\times 80}{100K\times 0.1}=1mH \end{matrix}\right\}. \quad (26)$$

The minimum value of C_2 with 0.01 % variation ratio of output voltage comes from:

$$\left\{\begin{matrix} \varepsilon=\dfrac{\Delta vo/2}{Vo}=\dfrac{1-d}{2RfC_2} \\ C_2=\dfrac{1-d}{2Rf\varepsilon}=\dfrac{1-0.5}{2\times 80\times 100K\times 0.01}=3.12\,\mu F \end{matrix}\right\}. \quad (27)$$

A modular DC-DC converter using cascaded boost converter of the proposed system is simulated using MATLAB SIMULINK program. The waveforms of i_{L1}, i_{L2}, i_{LS} and i_{Lo} are shown in Fig. 11 and V_{in}, V_{o1} and V_o in Fig. 12 respectively.

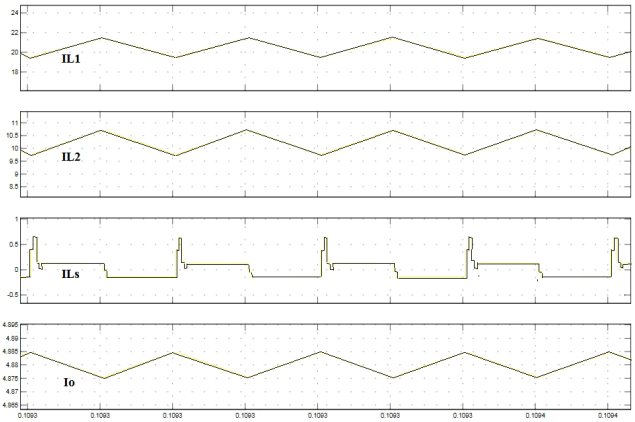


Fig. 11. I_{L1}, I_{L2}, I_{LS} and I_{Lo} Waveforms of proposed structure.

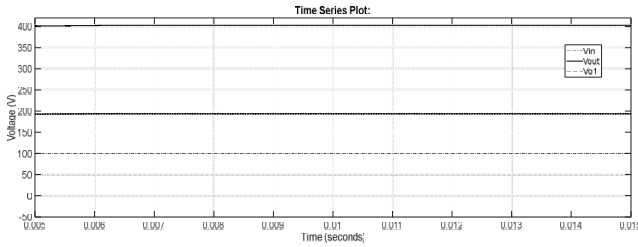


Fig. 12. V_{in}, V_{o1} and V_o Waveforms of the proposed structure with R = 100 ohm as output load.

Figure 13 also shows V_{in}, V_{o1} and V_o voltages for the inductive load, and the result shows the stability of the circuit for this type of loads. Figure 14 and Fig. 15 illustrate current wave forms of both proposed structures without and with inductive loads, and as can be seen there is no significant difference between these signals.

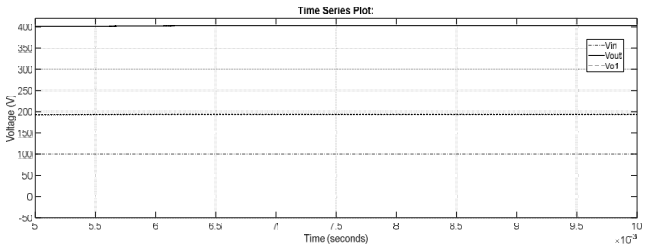


Fig. 13. V_{in}, V_{o1} and V_o Waveforms of proposed structure with R = 100 Ohm and L = 10 mH as output load.

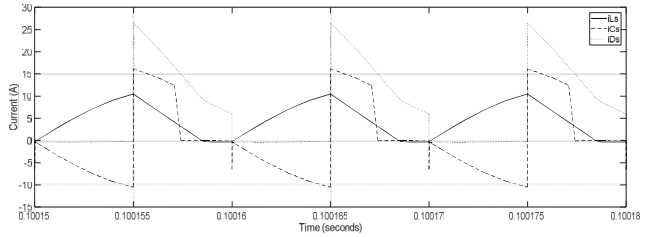


Fig. 14. Snubber inductor, capacitor and diode currents waveforms of proposed structure with R = 100 Ohm as output load.

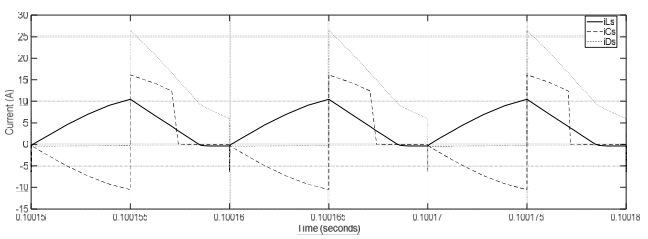


Fig. 15. Snubber inductor, capacitor an diode currents waveforms of proposed structure with R = 100 Ohm and L = 10 mH as output load.

In the final step, we have calculated the efficiency of the proposed structure in two different modes and have done a comparison with snuberless cascaded boost converter. Both conditions are given in Table II.

TABLE II. SIMULATION CONDITION FOR EFFICIENCY EVALUATION.

First step	Second step
$V_{in} = 100VDC$	$R_{Load} = 100\Omega$
$f_s = 100KHz$	$f_s = 100KHz$
$Duty - cycle = 0.5$	$Duty - cycle = 0.5$
$50\Omega \le R_{Load} \le 150\Omega$	$50VDC \le V_{in} \le 150VDC$

For this purpose, in the first step we fixed the input voltage at 100 VDC and calculated the efficiency according to changes of load. In the next step after fixing the load to 100 Ohms, we changed the input voltage from 50 VDC to 150 VDC and calculated the efficiency and as result it shows better results for both conditions because of smaller power switch losses for the proposed structure. Figure 16 shows the first condition and Fig. 17 shows results of the second condition.

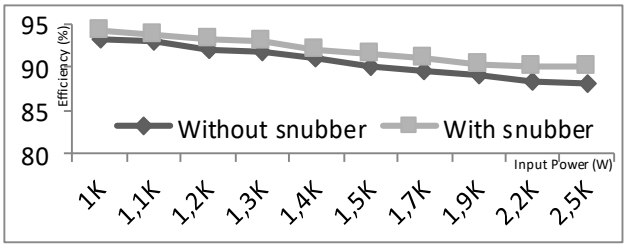


Fig. 16. Efficiency comparison in output powers from 1 KW to 2.5 KW between cascaded boost converter with snubber and without snubber circuit with fixed input voltage and variable load.

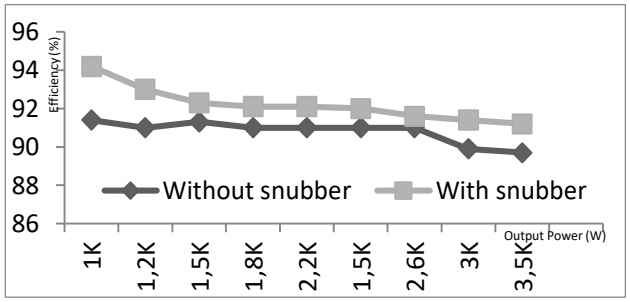


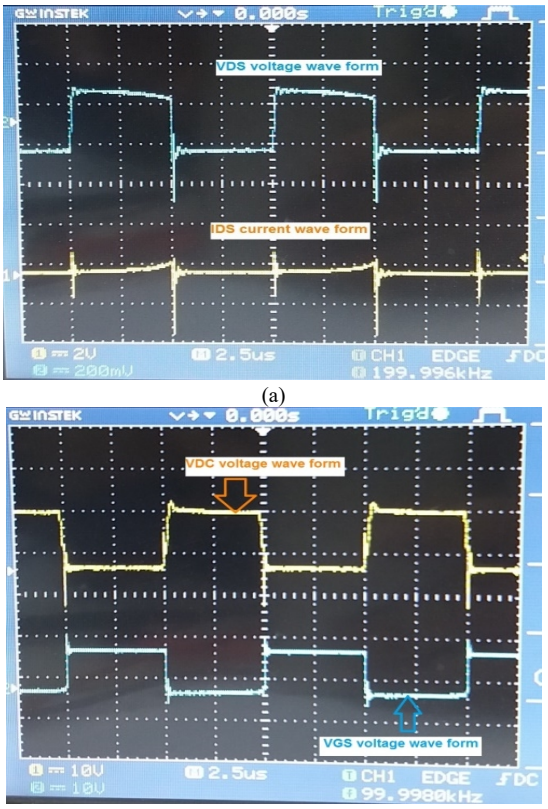
Fig. 17. Efficiency comparison in output powers from 1 KW to 3.5 KW between cascaded boost converter with snubber and without snubber circuit with fixed load and variable input voltage.

V. EXPERIMENTAL RESULTS

We implemented this structure in a laboratory scale with 100 Watt as output power. All parameters are selected by calculations above. As can be seen, we tested both structures at 100 KHz and 200 KHz as switching frequency. In Fig. 18, the drain-source voltage and current waveforms are given. For showing the results we adjusted scope *10 and *100 settings. Besides, this figure illustrates drain source and gate source voltage wave forms and it can be seen that when pulses receive gate-source pins, MOSFET switch goes into ON mode and otherwise it goes into OFF mode.

The most important subject is given in Fig. 19. Figure 19(a) shows switch turn off time when drain-source voltage goes from high level to low level and at the same

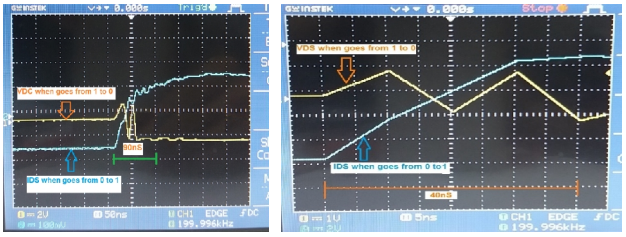
time the current that passes from the drain-source increases from low level to high level. As can be seen by applying the snubber sub-circuit to quadratic power boost converter this time has been very smaller regarding circuit without this sub-circuit. As can be seen from Fig. 19(b), this time changed from 90 ns to 40 ns and by this way according to Table I, T_{off1} is smaller and as a result losses are smaller.



(a)

(b)

Fig. 18. Drain-Source voltage and current wave forms (a), Drain-Source and Gate-Source voltage wave form (b).



(a) (b)

Fig. 19. V_{DS}-I_{DS} wave form when snubber sub-circuit is connected to converter (a); V_{DS}-I_{DS} wave form without snubber sub-circuit (b).

VI. Discussion

By using the concept of impedance matching between the resonant tank circuit and output capacitor, the circuit can drive heavy loads with high efficiency. Thus, by implementing soft switching, the voltage stress on the main switches is reduced, the losses are reduced and the ripples in the voltage and current waveforms are less. Furthermore, this structure uses two diodes, one inductor and one capacitor as snubber components and it is possible to apply it inexpensively. There is no need for an extra switch or a special resistor to remove the energy of the snubber capacitor. This study provides an advantage as it can point to more efficiency toward the structure without snubber circuit. High current stress on power switch during T_4 till T_5 and reverse recovery problems of diodes are among disadvantages of this structure.

VII. Conclusions

This study proposes a high frequency snubber circuit applied to cascaded boost converter with single power switch and shows that it can be effective in decreasing switching losses when it is in turn-off mode in high voltage applications. Simulations illustrate a better efficiency (2 % higher at 2 kW output power) with the desired output voltage. About the novelty of our study, it can be summarizing in several sections: using only one power switch in structure for high power transfer issue, simple and cheap elements application in circuit and ability to work in high frequency applications and quick reaction of proposed snubber sub-circuit. Simulations show that this structure reaches to about 390 VDC as output voltage, a result which is considered good given that 400 VDC is ideal. The time between high and low sides of voltage signal on power switch has decreased from 90 ns to 40 ns in 200 kHz.

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