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Comparative study of single-phase multilevel cascaded transformerless inverters with different modulation methods

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ABSTRACT

This paper presents an in-depth exploration of a single-phase multilevel cascaded H5 (CH5) transformerless inverter employing both phase-shifted PWM (PS-PWM) and level-shifted PWM (LS-PWM) methodologies. A comparative analysis is conducted with the conventional multilevel inverter (MLI) topologies, specifically the cascaded H-bridge (CHB) and H5 inverter configurations. The investigation delves into the impact of modulation index variations, load fluctuations, and modulation methods on the inverter's operational performance.

While switches in the CHB-MLI operate continuously at the carrier frequency state using PS-PWM and LS-PWM methods, the CH5-MLI exhibits a unique behavior with some switches toggling at high frequency, while others synchronize with the grid frequency. The CH5-MLI topology demonstrates efficiency improvements and a reduction in total harmonic distortion (THD). Notably, employing the LS-PWM method yields more significant efficiency enhancements and THD reduction compared to the PS-PWM method. To analyze power loss characteristics under diverse operating conditions, the PLECS simulation environment is leveraged for calculating conduction and switching losses.

The application of phase-shifted and level-shifted carrier-based pulse width modulation strategies to high and low-frequency switching switches results in minimized output harmonics, elevated operator safety, and enhanced overall reliability and efficiency. This work contributes significantly to the field by offering a detailed exploration of the CH5-MLI topology's dynamic behavior, modulation strategies, and their collective impact on performance metrics such as efficiency, THD, and power losses.

1. Introduction

Over time, our evolving world has imparted valuable lessons, equipping us with the knowledge and skills to navigate the challenges posed by a growing population and the finite nature of our energy resources. The escalating demand for energy, coupled with the adverse environmental impacts of conventional sources, has compelled a profound shift in our perspective on energy acquisition and utilization [1]. In response to these pressing concerns, renewable energy sources, including wind, solar (photovoltaic), hydropower, and ocean energy, have risen to the forefront as sustainable solutions, attracting considerable attention for their potential to address these challenges and deliver substantial benefits.

Photovoltaic (PV) is a highly promising renewable energy technology. The installation capacity and usage varieties of PV have been growing daily [2,3]. The converter used in the PV system plays a crucial role in transferring power from the PV to the consumer, utility, and grid. Depending on the galvanic isolation operation, the PV converter can be classified.

A grid frequency transformer provides galvanic isolation between the converter circuit side and the grid side. However, it increases the cost, weight, volume, and regular maintenance of the PV converter system while also reducing efficiency [4]. On the other hand, a transformerless structure improves efficiency, reduces filter size, and decreases the cost, weight, and volume of the PV converter. However, it can cause a dc current injection into the grid [5], generate ground leakage current due to parasitic capacitance in the PV system, and cause fluctuation in common-mode voltage[6,7]. Additionally, it can pose safety issues [8].

To minimize or suppress these undesirable effects caused by transformerless converters, various topology, modulation, and filter-based solutions have been proposed in the literature [9,10].

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A single-phase transformerless PV inverter topology can be categorized based on several factors. These include the number of input dc-link voltage (single, double, etc.) [11] and the fundamental origin of topology (H-bridge, NPC, etc.) [12]. Examples of these topologies include H5, HERIC, H6, H8, etc., which have a single dc-link voltage input and a two-level voltage output waveform [13,14]. While multilevel inverter architectures have been used in power system applications, particularly in high-voltage industrial and powertrain applications, for over two decades, commercial and residential scale PV converters based on the multilevel structure have only recently emerged [15,16].

A basic multilevel inverter (MLI) offers several advantages over a two-level inverter. It provides an output voltage with lower harmonic distortion, good modularity, less dV/dt voltage stress on devices, and reduced losses. These benefits enhance the system's reliability and lifespan, decrease the size of the filter, and improve the voltage quality [17,18]. The common MLI topologies can be classified as neutral-point clamped (NPC), cascaded H-bridge (CHB), and custom/modified [15,19,20].

A single-phase NPC converter generally has less ground leakage current compared to other converters [16]. However, it requires twice the dc-link voltage of the CHB topology. An insulated power supply is necessary for CHB converter topologies. An unequal/unbalanced power supply or PV output voltage can impact the converter's modularity, efficiency, reliability, and stability. On the other hand, the CHB converter has advantages such as a simple structure, easy-to-increase output voltage level, and a requirement for only unidirectional switches [21]. Custom/modified converters are based on other conventional MLI topologies and aim to reduce the number of switches and achieve higher output voltage levels [22,23]. These topologies offer cost and space savings, as well as a lower component count. However, they often require custom modulation and control strategies [21].

A single-phase 19-level asymmetric cascaded inverter is discussed with Lyapunov-based model predictive control to reduce the harmonic distortion and the number of switches. This topology consists of three full-bridge switches and three asymmetric dc voltage sources [24]. Additionally, to minimize voltage ripple in the dc link capacitor, improve waveform quality, achieve lower capacitor voltage ripple, and ensure more uniform power distribution, a single-phase 9-level cascaded inverter with modified phase disposition pulse width modulation (PD-PWM) control is proposed. This topology utilizes four full-bridge switches and four symmetric dc voltage sources [25].

An analysis is conducted on a single-phase trinary asymmetrical CHB (TACHB) inverter with a level doubling network (LDN) using the phase disposition level shift pulse width modulation (PD-LSPWM) technique. The objective is to achieve a 17-level output voltage waveform with low total harmonic distortion (THD) while minimizing the number of dc sources. The system consists of 12 switches, a capacitor, and two asymmetrical dc sources. It includes two H-bridges (each with four switches and a dc source) and an LDN (four switches and a capacitor). Simulation and experimental studies have been performed [26]. Additionally, a single-phase nine-level trinary dc source fed cascaded H-bridge inverter with a modified carrier-based level shifted-phase disposition pulse width modulation (LS-PDPWM) technique is discussed. The system comprises two H-bridges (each with four switches, one with a dc source, and the other with three times the dc source). Simulation and experimental tests have been conducted to evaluate the system's performance in standalone and grid-connected scenarios [27].

A simulation test is conducted to investigate a single-phase 13-level standalone cascaded multilevel inverter. The inverter is composed of three H-bridges, each with four switches and a dc source, and one half-bridge, each with two switches and a half dc source. The phase opposition disposition carrier arrangement with PWM (POD-PWM) is used as the modulation technique. A comparison is made between the conventional CHBMLI and the proposed cascaded MLI based on various factors such as switches, dc sources, power losses, etc. The study demonstrates that the proposed topology has fewer components, lower power losses, and lower THD [28].

The Interconnection and damping assignment passivity-based control (IDA-PBC) strategy is a nonlinear controller that uses the phase-shifted PWM (PS-PWM) method. It is employed for a single-phase seven-level CHB inverter, which consists of three full-bridge switches and three symmetric dc voltage sources. This document provides a detailed description of the controller through simulation and experimental investigations under different conditions such as normal operation, grid voltage sag and swell, and uneven irradiance [29].

To address the power imbalance between CHBs, a power matching approach is used for an eleven-level CHB inverter with the PS-PWM method. The topology consists of five CHBs, and simulation and experimental studies are conducted to maintain unit power factor operation, resolve power mismatch issues, and overcome overmodulation [30].

For a 5-level CHB inverter with two full-bridge switches, the PS-PWM strategy combined with the normalized Huber adaptive control algorithm is employed to mitigate reactive power and harmonics. Simulation and experimental investigations are carried out under various conditions such as load variations, voltage sag and swell, and distorted grid. A comparison study is performed between the normalized Huber algorithm and conventional algorithms such as least mean square (LMS), recursive least squares (RLS), and synchronous reference frame theory (SRFT), considering different aspects such as type of filter, weight estimation, total harmonic distortion (THD) of supply current, steady-state error, convergence, complexity, and sampling time [31].

A simulation and experimental tests are conducted to discuss a single-phase seven-level CHB inverter with two proposed improved PWM techniques. These techniques aim to balance the power between modules, reduce switching losses, and improve efficiency in a standalone scenario. The study includes a comparison with three known modulation methods. In this system, there are three H-bridges, each consisting of four switches and a dc source [32]. Additionally, a single-phase seven-level CHBMLI topology is proposed to control power and battery management in a standalone solar PV system. This topology consists of three full-bridge switches and three symmetric dc voltage sources [33].

An analysis is conducted on a single-phase two-bridge CHB multilevel inverter (CHBMLI) using the selective harmonic mitigation pulse width modulation (SHM-PWM) technique. The goal is to improve the quality of the output voltage for both constant and variable two isolated dc sources that feed the single-phase CHBMLI. By increasing the voltage levels (from 5 to 9) and adjusting the switching angles (from 6 to 12), an increase in output voltage quality and a reduction in voltage distortion are observed. The simulation and experimental results demonstrate the achievement of high-quality voltage [34].

Additionally, a proposal is made for a single-phase 9-level CHB inverter (consisting of four full-bridges) using the selective harmonic elimination PWM (SHE-PWM) technique in standalone mode. This proposal aims to maintain a constant fundamental component of the output voltage while eliminating the third, fifth, and seventh order harmonics [35].

Simulation investigation is conducted to test single-phase standalone 7, 9, and 11-level CHB inverters using the SHE method. These inverters are equipped with three, four, and five full-bridge switches, respectively. To eliminate low-order harmonics in the system, optimization techniques such as Dragonfly Algorithm (DA), Particle Swarm Optimization (PSO), Accelerated Particle Swarm Optimization (APSO), Differential Evolution (DE), and Grey Wolf Optimization (GWO) are used to optimize switching angles. The test results indicate that no single algorithm demonstrates complete dominance in all scenarios [36].

The various topologies associated with PV applications discussed above come with their own set of advantages and disadvantages. This study focuses on a single-phase cascaded H5 transformerless PV inverter topology. The cascaded configuration employs two well-established transformerless H5 inverters to generate seven output voltage levels. This inverter comprises ten unidirectional controllable power switches,

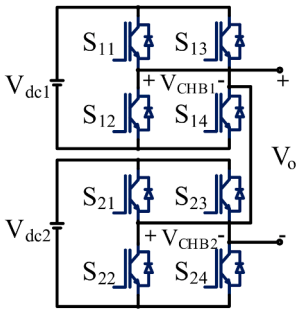


Fig. 1. Schematic of 5-level CHBMLI.

with six switches operating at the carrier frequency and four at the grid frequency. The high and low-frequency switching switches utilize phase-shifted and level-shifted carrier-based pulse width modulation strategies. The system's topology, along with these modulation strategies, results in reduced output harmonics, enhanced operator safety, and improved overall reliability and efficiency.

The remaining sections of the paper are organized as follows: Section II discusses the inverter topologies, their working principles, modulation methods, and power loss calculation. Next, in Section III, the inverter topologies with different modulation methods are tested under various test conditions using the MatLab/Simulink platform and PLECS software, and the simulation results are presented. Finally, Section IV provides the conclusion for the inverter topologies.

2. Method

2.1. Cascaded H-bridge multilevel inverter

A cascade H-bridge multilevel inverter (CHBMLI) consists of H-bridge inverters connected in series to produce multilevel ac voltage. The conventional 5-level CHBMLI topology is shown in Fig. 1.

5-level CHB consists of two H-bridge inverters and two dc sources. Here, the output voltage level (m) is as in Eq. (1).

$$m = (2n+1) \tag{1}$$

where n is the number of dc sources. This topology comprises two H-bridges switches ($\{S_{11}, S_{12}, S_{13}, S_{14}\}$ and $\{S_{21}, S_{22}, S_{23}, S_{24}\}$) supplied by two dc sources (V_{dc1} and V_{dc2}).

The switches are managed by a complementary pair strategy, which is based on $\overline{S}_{i1} = S_{i2}$ and $\overline{S}_{i3} = S_{i4}$ and generalized switch stated can be presented as follows:

$$S_{ij} = \begin{cases} 1 & \text{If it is closed} \quad (\overline{S}_{ij} \text{ is opened}) \\ 0 & \text{If it is opened} \quad (\overline{S}_{ij} \text{ is closed}) \end{cases} \tag{2}$$

where $i = 1, 2$ and $j = 1, 2$. To generate five voltage levels ($+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$,) in CHB inverter, there are five different switching states. These states are given in Table 1. For example, S_{11}, S_{14}, S_{21} and S_{24} switches must be ON, S_{12}, S_{13}, S_{22} and S_{23} switches must be OFF to obtain $+2V_{dc}$ voltage level according to Table 1, indicating the dc sources are symmetrical ($V_{dc1} = V_{dc2} = V_{dc}$).

The switching states can be used to yield an output voltage equation.

If the switching rule is assumed as follows:

$$S_i = S_{i1} - S_{i3}, \; i = 1, 2 \tag{3}$$

where S_i denotes the switching rule of the i th H-bridge. The output terminal voltage V_o can be written by using Table 1 and Eq. (3) as follows:

$$v_o = S_1 V_{dc} + S_2 V_{dc} \tag{4}$$

2.2. H5 inverter

The H5 inverter topology consists of adding a fifth switch to the basic H-bridge inverter. The H5 inverter topology is shown in Fig. 2.

S_1 and S_3 switches are switched at grid frequency in H5 inverter while S_2, S_4 and S_5 are switched at the carrier frequency. Table 2 shows

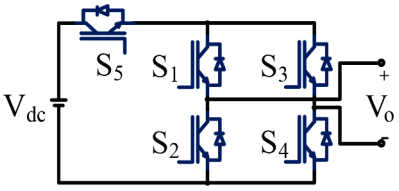


Fig. 2. Schematic of H5 inverter.

Table 2
H5 inverter switching states and terminal voltages.

Level	State	S_1	S_2	S_3	S_4	S_5	V_o
1	1	1	0	0	1	1	$+V_{dc}$
2	2	1	0	0	0	0	0
3	3	0	1	1	0	1	$-V_{dc}$
2	4	0	0	1	0	0	0

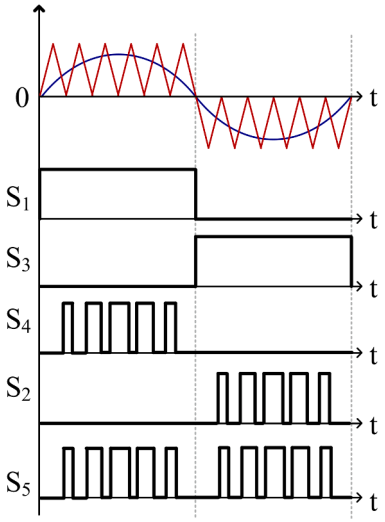


Fig. 3. H5 inverter switching signals.

Table 1
5-Level CHBMLI switching states and terminal voltages.

Level	State	S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}	V_{CHB1}	V_{CHB2}	V_o
1	1	1	0	0	1	1	0	0	1	V_{dc}	V_{dc}	$+2V_{dc}$
2	2	1	0	0	1	0	1	0	1	V_{dc}	0	$+V_{dc}$
3	3	1	0	1	0	0	1	0	1	0	0	0
4	4	1	0	1	0	0	1	1	0	0	$-V_{dc}$	$-V_{dc}$
5	5	0	1	1	0	0	1	1	0	$-V_{dc}$	$-V_{dc}$	$-2V_{dc}$

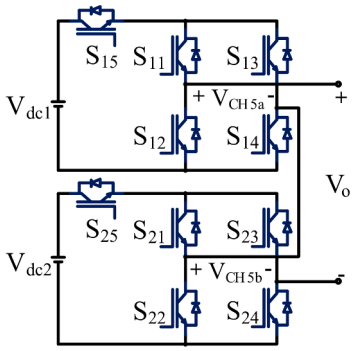


Fig. 4. Schematic of 5-level CH5MLI.

the H5 inverter switching states. Fig. 3 shows the PWM switching signals of the H5 inverter switches.

2.3. Cascaded H5 multilevel inverter

A cascaded H5 multilevel inverter (CH5MLI) comprises H5 inverters connected in series to produce multilevel ac voltage. The 5-level CH5MLI topology is shown in Fig. 4.

CH5MLI inverter output voltage levels can be increased by adding the dc sources as in traditional CHB inverter. In the literature, only directly related to one study has been done about CH5MLI [37]. In [37], the proposed CHMLI has a 5-level output voltage and all switches switch at the carrier frequency. However, in this study, while four switches (S_{11}, S_{13}, S_{21} and S_{23}) of the CH5MLI are switched at grid frequency, six switches (S_{12}, S_{14}, S_{15}, S_{22}, S_{24} and S_{25}) are switched at carrier frequency. The switching states of CH5LMI is given in Table 3.

This switching strategy helps to reduce the power losses in CH5MLI. Phase-shifted PWM (PS-PWM) and level-shifted PWM (LS-PWM) modulation techniques are applied to CH5MLI in this study. The implementation of the modulation techniques is realized by the generating pulses produced by the logic gates shown in Fig. 5.

All triangular carriers have the same frequency and peak-to-peak amplitude in PS-PWM (Fig. 6(a)). Therefore, a phase shift exists between two adjacent carrier waves, as expressed in Eq. (5).

$$\phi_{cr} = 2\pi/N \tag{5}$$

where N is a number of cascaded inverter structures; in the LS-PWM technique, if the multilevel inverter has m levels, $m-1$ carrier signals are required. Here, carrier signals are vertically placed. In this case, four triangle carrier signals generate a 5-level output voltage.

Fig. 6(b) shows that the carrier signals' magnitude ranges from 1 to 0.5, 0.5 to 0, 0 to −0.5, and −0.5 to −1. The switching pulses of the 5-level CH5MLI system are also shown in Fig. 6(b).

The switching signal of S_{15} is the sum of the switching signals S_{14} and S_{12}, and the switching signal of S_{25} is the sum of the S_{24} and S_{22} switching signals as follows:

$$S_{15} = S_{12} + S_{14} \tag{6}$$

$$S_{25} = S_{22} + S_{24} \tag{7}$$

Each topology comprises variant components and types to produce desired voltage level on the output of the inverter. The number of components needed to produce 5-level voltage output related to the topology is given in Table 4.

2.4. Power loss calculation and analysis

Power loss can be majorly classified as conduction and switching losses. While conduction loss is more dominant at the low switching frequency, switching loss is more effective at the high switching frequency. Based on the inverter topologies, a unidirectional IGBT switch and connected antiparallel diode should be considered to calculate the losses [26,28,32,38]. The conduction losses of each component (IGBT and diode) can be calculated as given below:

$$P_{Conduction\ Loss\ (diode)}(t) = V_{diode}(t) + R_{diode} i^2(t) \tag{8}$$

$$P_{Conduction\ Loss\ (IGBT)}(t) = V_{IGBT}(t) + [R_{IGBT} i^{\alpha}(t)\,]i(t) \tag{9}$$

where V is an on-state voltage, R is a resistance, and α is a constant related to the characteristics of the IGBT switch.

The states of the switch are used to determine switching losses. The switching losses consist of on-state losses and off-state losses as follows:

$$P_{Switching\ Loss} = P_{Switching\ Loss(ON)} + P_{Switching\ Loss(OFF)} \tag{10}$$

The ON-state and OFF-state switching losses can be defined as:

$$P_{Switching\ Loss\ (ON)} = \frac{1}{T_{sw}} \int_0^{t_{ON}} \left(\frac{V_{IGBT}}{t_{ON}} t\right)\left(-\frac{I_{sw}}{t_{ON}}(t - t_{ON})\right) dt \tag{11}$$

$$P_{Switching\ Loss\ (OFF)} = \frac{1}{T_{sw}} \int_0^{t_{OFF}} \left(\frac{V_{IGBT}}{t_{OFF}} t\right)\left(-\frac{I_{sw}}{t_{OFF}}(t - t_{OFF})\right) dt \tag{12}$$

where T_{sw} is a total switching period, t_{ON} and t_{OFF} are the ON-state and OFF-state periods of the IGBT switch, respectively. V_{IGBT} and I_{sw} are the actual voltage and current values of the IGBT switch, respectively.

The power losses of the inverter topologies are calculated using Piecewise Linear Electrical Circuit Simulation (PLECS) software with the IGBT switch and diode switch models F3L30R06W1E3_B11 with their

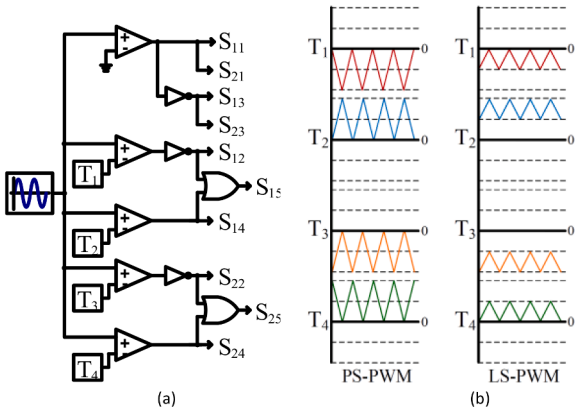


Fig. 5. (a) Logic gates for modulation techniques (b) Carrier waveforms for PS and LS-PWM.

Table 3
5-Level CH5MLI switching states and terminal voltages.

Level	State	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	S_{21}	S_{22}	S_{23}	S_{24}	S_{25}	V_{CH5a}	V_{CH5b}	V_o
1	1	1	0	0	1	1	1	0	0	1	1	V_{dc}	V_{dc}	$+2V_{dc}$
2	2	1	0	0	1	1	1	0	1	0	0	V_{dc}	0	$+V_{dc}$
3	3	1	0	1	0	0	1	0	1	0	0	0	0	0
4	4	1	0	1	0	0	0	1	1	0	1	0	$-V_{dc}$	$-V_{dc}$
5	5	0	1	1	0	1	0	1	1	0	1	$-V_{dc}$	$-V_{dc}$	$-2V_{dc}$

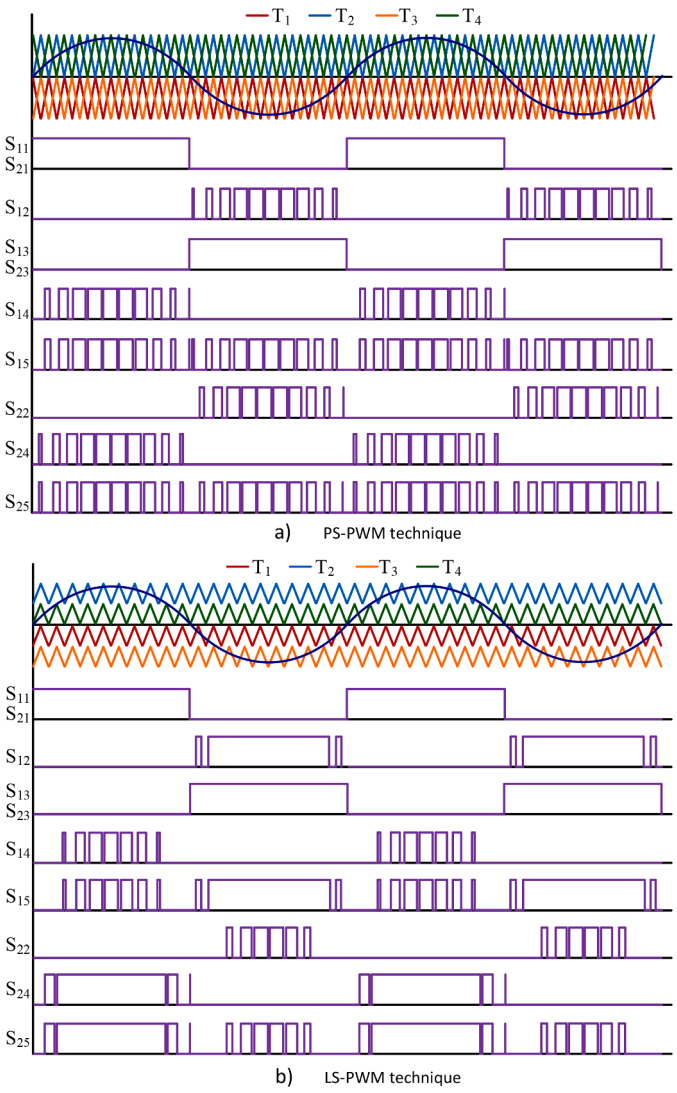


Fig. 6. PWM switching strategy for 5-level CH5MLI. (a) PS-PWM and (b) LS-PWM.

Table 4
Comparison of variant 5-level MLI topologies.

Component required	NPC	DC	FC	CHB	CH5
Switch (carrier frequency)	8	8	8	8	6
Switch (grid frequency)	0	0	0	0	4
DC source	1	1	1	2	2
DC link capacitor	4	3	3	0	0

switching characteristics. In PLECS, conduction and switching losses are determined through the utilization of look-up tables related to the switches. These tables serve as references, and actual losses are computed during simulations by employing linear interpolation when the input values, such as on-state current, pre- and post-switching current or voltage, and junction temperature, fall within the specified index range. If an input value exceeds the defined range, PLECS resorts to extrapolation, utilizing the first or last pair of index values. The ambient temperature is assumed to be constant and uniformly distributed at 25°C. The means of the periodic and impulse average methods calculate the conduction and switching losses. The loss model for the IGBT switch F3L30R06W1E3_B11 is shown in Fig. 7.

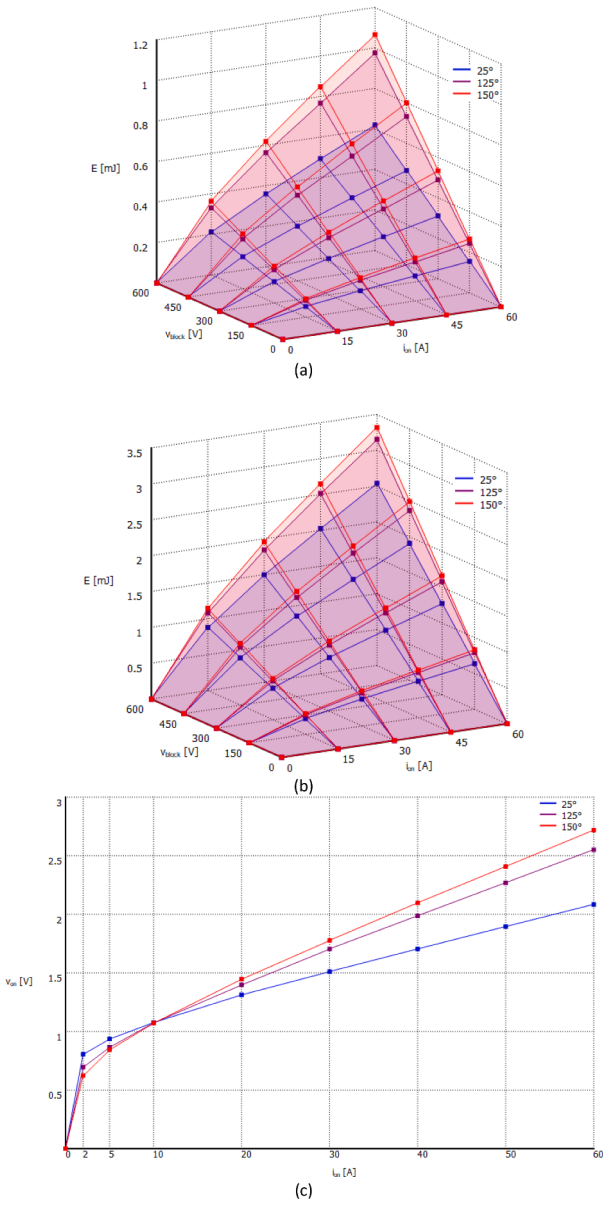


Fig. 7. Loss model for (a) turn ON losses, (b) turn OFF losses, and (c) conduction losses for IGBT F3L30R06W1E3_B11 up to 60A, [E = Energy loss (mJ), Vblock = OFF state blocking voltage (V), ion = ON state current (A), and Von = ON state voltage drop (V)].

Table 5
Parameter used for simulation studies.

Parameter	Value
DC source voltage	$V_{dc1} = V_{dc2} = 175.8\,\text{V}$, $V_{dc} = 300.65\,\text{V}$
Load	$R = 40 - 800\,\Omega$
Modulation index	$m_i = 0 - 1.0$
Carrier (Switching) frequency	$f_{carrier} = 0.5 - 20\,\text{kHz}$
Grid (Reference) frequency	$f_{ref} = 50\,\text{Hz}$
Switch	$R_{on} = 1\,\text{m}\Omega$, $L_{on} = 0\,\text{mH}$, $V_f = 1.45\,\text{V}$

3. 3. Simulation findings

The inverter configurations with modulation techniques are designed and simulated in MatLab/Simulink platform. CHBMLI, CH5MLI and H5 topologies with sinusoidal pulse width modulation (SPWM), PS-PWM and LS-PWM techniques are used in simulation

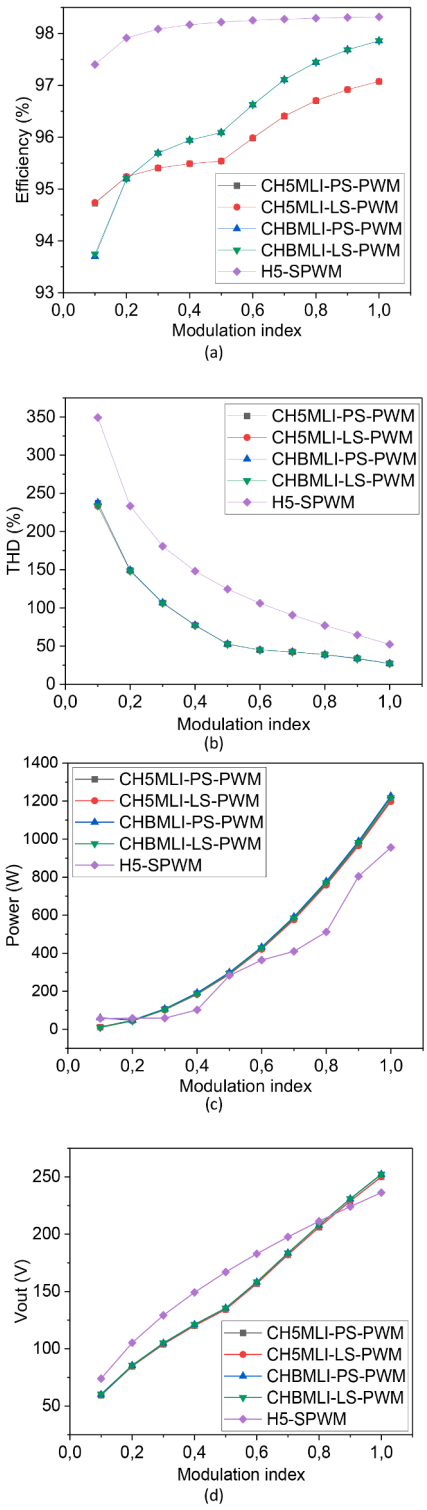


Fig. 8. Graphical representation of (a) modulation index versus efficiency, (b) modulation index versus % THD, (c) modulation index versus output power, (d) modulation index versus output voltage.

studies. The system parameters are given in Table 5.

The efficiency (η) of the inverters is calculated as $\eta = P_{out}/P_{in}$ by measuring the input power (P_{in}) and the output power (P_{out}). The efficiency, THD, output power and voltage variations depending on the modulation index varying from 0.1 to 1.0 are shown in Fig. 8. During the simulation, carrier frequency ($f_{carrier}$) is 20 kHz, and load (R) is 48.4 Ω.

Increasing the modulation index causes to increase in each efficiency

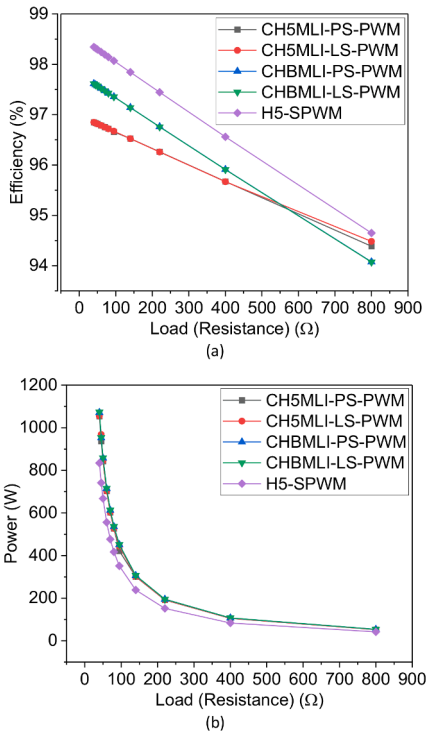


Fig. 9. Graphical representation of (a) load versus efficiency, (b) load versus output power.

of the inverters, as shown in Fig. 8(a). Efficiency variation is between about 97.402 % and 98.319 % in H5, 94.724 % and 97.075 % in CH5MLI and 93.701 % and 97.859 % in CHBMLI topologies. During the lowest modulation index condition, efficiency with CHBMLI topology has a lower value than CH5MLI and H5 topologies. After that condition, the efficiency with CHBMLI is higher than CH5MLI. The efficiency of the H5 topology is always better than the other topologies. The topology with the LS-PWM technique shows better performance than the PS-PWM. Increasing the modulation index produces a higher output voltage amplitude when the load is constant. Thus, the output current value and related power losses also rise. While similar voltage and current are observed at the output of the inverters, more power losses are seen where the number of switches/components is higher. The main result is that the H5 inverter system has higher efficiency characteristics, as shown in Fig. 8(a).

Increasing the modulation index results in improved output voltage and current waveforms and less THD in current, as shown in Fig. 8(b). THD variation is between about 349.17 % and 52.36 % in H5, 233.24 % and 27.18 % in CH5MLI, and 233.73 % and 27.18 % in CHBMLI topologies. THD values are higher than the standard values because the topologies' outputs are directly connected to the load. If the filters such as LC, LCL, etc. structures are used at the end of the inverter topologies, the THD values will decrease. But this study discusses the topologies without filter structure with different modulation techniques. MLI topologies exhibit better characteristics regarding THD than the H5 topology. While the modulation index increases, the output voltage levels become apparent, and the voltage waveforms come closer to sinusoidal forms. Here, MLI topologies unveil similar behaviour, and the topology with LS-PWM technique performs better than the PS-PWM.

The output voltage, current and power values increase with the incremental modulation index and constant load, as shown in Fig. 8(c). In the MLI topologies, the modulation index has a crucial role in building voltage levels. Decreasing the modulation index can cause the voltage level to disappear. On the other hand, increasing the modulation index can provide the voltage level appearing, higher voltage value and more stable power at the end of the ML.

Table 6
5-Level CH5MLI switching states and terminal voltages.

Harmonics order	H5	CH5MLI		CHBMLI	
	SPWM	PS-PWM	LS-PWM	PS-PWM	LS-PWM
3rd	5.77	0.48	0.37	0.48	0.38
5th	0.71	0.02	0.06	0.02	0.06
7th	0.44	0.05	0.11	0.04	0.10
9th	5.14	0.07	0.01	0.06	0.01
11th	6.53	0.05	0.06	0.05	0.05
13th	4.31	0.01	0.07	0.01	0.07
15th	6.25	0.01	0.04	0.01	0.04
17th	0.32	0.03	0.03	0.03	0.03
19th	3.26	0.01	0.04	0.02	0.04
Total	70.43	36.52	36.59	36.52	36.59

In MLI topologies, as the modulation index is raised from 0.5 to 1.0, the output voltage value increases more linearly than the H5 topology, as shown in Fig. 8(d). On the other hand, there are two dc sources in the MLI and one dc source in the H5, so the output voltage values and characteristics can differ.

The efficiency and output power variations depending on the load varying from 40 Ω to 800 Ω are shown in Fig. 9. During the simulation, carrier frequency ($f_{carrier}$) is 20 kHz, and the modulation index (m_i) is 0.85.

While input dc voltage sources' values, modulation index and carrier frequency are constant and the output load value is varied from 40 Ω to 800 Ω, the system efficiency is observed to be dependent on the topology types, as depicted in Fig. 9(a). Efficiency variation is between 94.650 % and 98.343 % in H5, 94.484 % and 96.848 % in CH5MLI, and 94.078 % and 97.617 % in CHBMLI topologies.

When the load value is low, the output current value is high, and the current is low when the load is high. While the inverter output current consumption is high, the power loss in the inverter having more components/switches, such as CHBMLI and CH5MLI, is higher and lower for the inverter containing components/switches, such as H5, and thereupon efficiency with H5 inverter is higher than the CHBMLI and CH5MLI. But the load value is high for low power consumption, the output current is low, and the CH5MLI topology shows better efficiency characteristics than the CHBMLI topology. On the other hand, the ranges of variation in efficiency from largest to smallest are H5, CHBMLI and CH5MLI, respectively, and therefore it can be stated that the CH5MLI exhibits robust characteristics in terms of the efficiency variation aspect.

Although the modulation index, carrier frequency and input dc voltage sources are constant, the output power values are different against each other in the topologies due to the differences in the output voltage values as depicted in Fig. 9(b). As a result, the output power versus the load exhibits exponential characteristics.

The output current harmonic components based on the topologies and modulation techniques are given in Table 6.

During the simulation, carrier frequency ($f_{carrier}$) is 20 kHz, modulation index (m_i) is 0.85, and load (R) is 48.4 Ω. The THD characteristics of the MLI topologies are better than the H5 topology. The total THD values are higher than the typical values (IEEE 1547, IEC 61727) since there is no filter at the end of the inverter topologies, and the load is purely resistive. Besides, the CH5MLI and CHBMLI topologies with PS-PWM and LS-PWM techniques have almost the same THD behaviours.

Fig. 10 shows CH5MLI with LS-PWM system simulation for different operation conditions as modulation index (m_i) and frequency variations for a constant load.

The output voltage waveform for the variation of m_i from 0.35 to 0.55 with the constant load ($R = 48.4\,\Omega$) is depicted in Fig. 10(a), and the FFTs of the output voltage related to the modulation index are shown in Fig. 10(b) and 10(c). Fig. 10(d) shows the output voltage waveform for the variation of m_i from 0.90 to 0.65 with the constant load ($R = 48.4\,\Omega$), and Fig. 10(e) and 10(f) depict the FFTs of the output voltage.

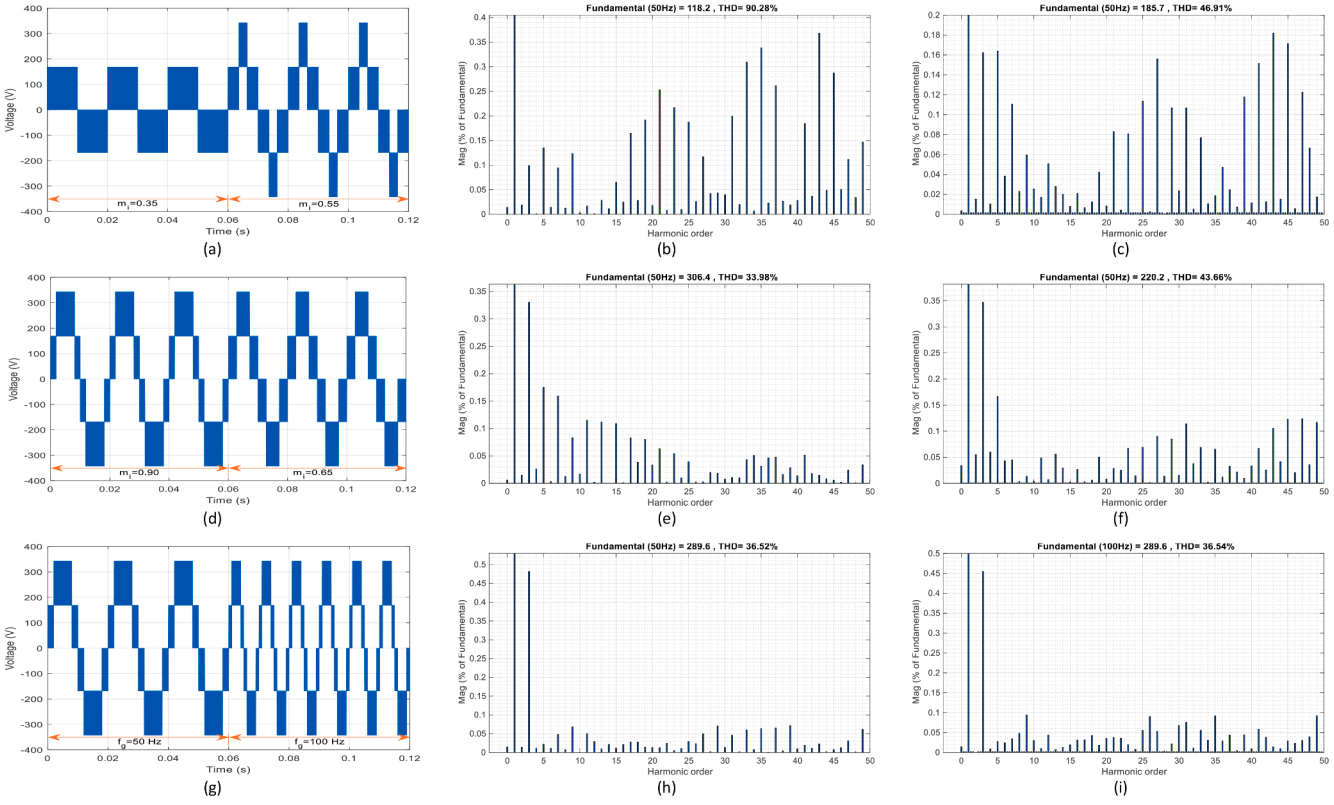
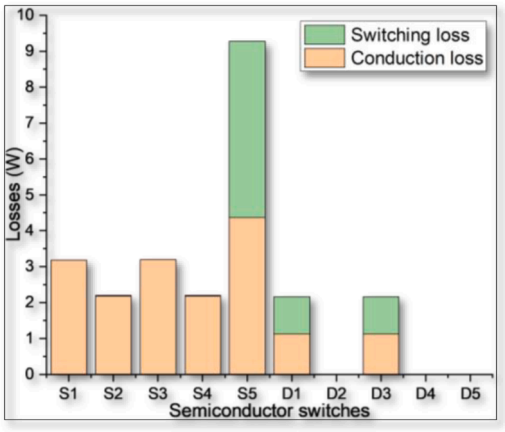
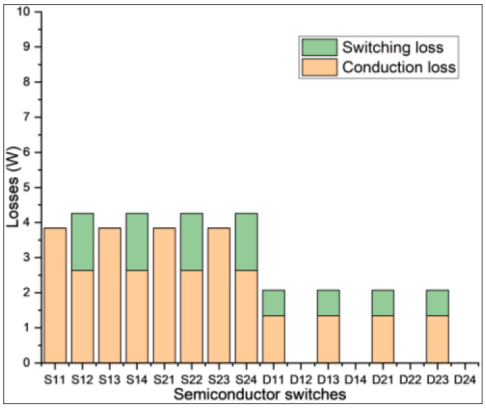


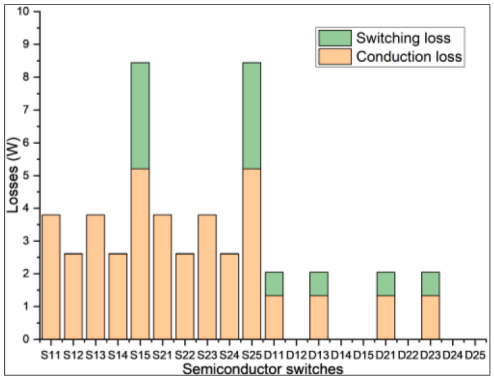
Fig. 10. Simulation result. (a) modulation index variation ($m_i = 0.35$ to $m_i = 0.55$). (b) voltage FFT ($m_i = 0.35$). (c) voltage FFT ($m_i = 0.55$). (d) modulation index variation ($m_i = 0.90$ to $m_i = 0.65$). (e) voltage FFT ($m_i = 0.90$). (f) voltage FFT ($m_i = 0.65$). (g) Grid (reference) frequency variation ($f = 50$ Hz to $f = 100$ Hz). (h) voltage FFT ($f = 50$ Hz, $m_i = 0.85$). (i) voltage FFT ($f = 100$ Hz, $m_i = 0.85$).



(a)



(b)



(c)

Fig. 11. Power loss distribution of the inverters in the semiconductor switches. (a) H5 inverter (b) CHBMLI (c) CH5MLI [$m_i = 0.85, f_{sw} = f_{carrier} = 20\,\text{kHz}, f = 50\,\text{Hz}, V_{dc1} = V_{dc2} = 175.8\,\text{V}, V_{dc} = 300.65\,\text{V}, R_{load} = 25\,\Omega, L_{load} = 5\,\text{mH}$].

The variation of the output voltage frequency from 50 Hz to 100 Hz with the constant load ($R = 48.4\,\Omega$) is observed as shown in Fig. 10(g), and the related FFTs are depicted in Fig. 10(h) and 10(i).

PLECS software is used to attain the loss of the topologies. The power loss distribution of different switches related to the inverter topologies is shown in Fig. 11.

The turn-on loss of the body diode is ignored, and turn-off and conduction losses of the body diode are considered in this study. From the results in Fig. 11(a), total switching and conduction losses are about 7.00 W and 17.40 W, respectively. Each switch has conduction and switching losses. Due to the fact that S_1 and S_3 switches are switched at grid frequency and S_2, S_4 and S_5 are switched at the carrier frequency, switching losses belonging to S_1 and S_3 switches are lower than others and are not observed clearly in the chart. S_5 switch has the highest switching loss since S_5 is switched at carrier frequency during the entire grid frequency period and S_2 and S_4 switches with a half period of the grid frequency. The total power loss of the H5 inverter is observed as 24.40 W. From the results in Fig. 11(b), the total power loss of CHBMLI is about 40.68 W, the switching loss part is about 9.40 W, and the conduction loss part is about 31.28 W. PS-PWM modulation technique is applied to the CHBMLI, and during the half period of grid frequency, S_{11}, S_{13}, S_{21} and S_{23} switches are ON-state position and S_{12}, S_{14}, S_{22} and S_{24} switches are OFF-state position, and also, the other half of the period of grid frequency, and all switches operate at the carrier frequency. Therefore, as the conduction losses are dominant on S_{11}, S_{13}, S_{21} and S_{23} switches, the switching losses bring themselves into the forefront on S_{12}, S_{14}, S_{22} and S_{24}.

From the results in Fig. 11(c), the total power loss of CH5MLI with PS-PWM is about 50.71 W, the switching loss part is about 9.36 W, and the conduction loss part is about 41.35 W. While S_{11}, S_{13}, S_{21} and S_{23} switches are switched at grid frequency, S_{12}, S_{14}, S_{22} and S_{24} switches are OFF-state position during the half period of grid frequency and are switched at carrier frequency during the other half period of grid frequency; therefore, the conduction losses are dominant for all these switches. On the other hand, S_5 is switched at carrier frequency during the entire grid frequency period, and this causes S_5 switch to have the highest switching and conduction losses of all switches.

The topology structures of the CHBMLI and CH5MLI have similarities, as shown in Figs. 1 and 4. The CH5MLI also has an H-bridge part, as in the CHBMLI, with a different switching strategy, from PS-PWM method. If only H-bridge part switches (S_{11}, S_{12}, S_{13}, S_{14}, S_{21}, S_{22}, S_{23}, S_{24}) are compared with loss aspects, both conduction and switching losses can be determined to be lower at the H-bridge part in CH5MLI than in the CHBMLI. S_{25} switch has the highest conduction and switching losses, which causes the total loss in CH5MLI to be higher than the CHBMLI.

Fig. 12 shows the loss distribution of the inverter topologies at varying operating conditions.

Power losses distribution versus modulation index variation ($m_i = 1.0$ to $m_i = 0.6$) for the inverter topologies is shown in Fig. 12(a). Both conduction and switching losses decrease with a reduction in modulation index values. However, the modulation index reduction causes the share of switching loss in a total loss to increase. Variation of switching and conduction loss share in a total loss is more limited with CH5MLI topology.

Switching (carrier) frequency variation ($f_{sw} = 5$ to $f_{sw} = 20\,\text{kHz}$) brings about an increase in switching losses and almost no change of conduction loss, as shown in Fig. 12(b). Conduction losses are more dominant than switching losses, and switching loss with CH5MLI is always lower than CHBMLI for modulation index and frequency variation operation conditions, as shown in Fig. 12(a) and 12(b).

When the output load value is increased, the consumed current value decreases, and then power losses related to the conduction and switching also drop off, as shown in Fig. 12(c). It is because the conduction loss share, which is more dominant than the switching, lessens with an increment of the load value.

4. Conclusion

This paper has presented a comprehensive analysis of a single-phase seven-level cascaded H5 transformerless inverter utilizing both phase-shifted PWM (PS-PWM) and level-shifted PWM (LS-PWM) methods. Our proposed multilevel inverter structure, CH5MLI, has been demonstrated to significantly enhance the overall level of total harmonic distortion, particularly when subjected to high-voltage applications where the current value is relatively smaller than in low-voltage scenarios.

The performance evaluation of the CH5MLI has revealed noteworthy improvements in efficiency with low current consumption, achieved

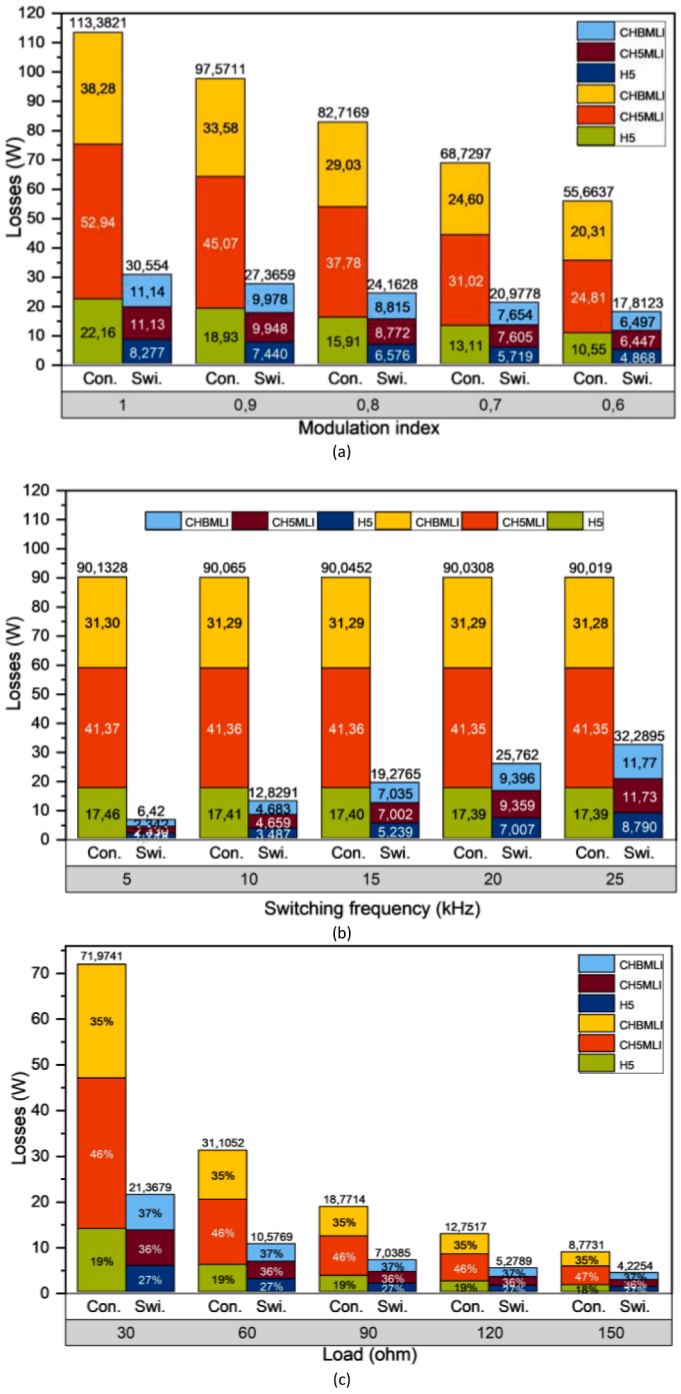


Fig. 12. Power loss for different conditions (a) modulation index variation ($m_i = 1.0$ to $m_i = 0.6$) (b) switching (carrier) frequency variation ($f_{sw} = 5$ to $f_{sw} = 20\,\text{kHz}$) (c) load variation ($R_{load} = 50$ to $R_{load} = 140\,\Omega$) [$f = 50\,\text{Hz}$, $V_{dc1} = V_{dc2} = 175.8\,\text{V}$, $V_{dc} = 300.65\,\text{V}$, $L_{load} = 5\,\text{mH}$].

through the strategic implementation of PS-PWM and LS-PWM methods. It is evident from our findings that the CH5MLI topology excels in maintaining a robust efficiency profile even amidst load changes, showcasing its suitability for applications with varying load conditions.

In the context of modulation index variation, the LS-PWM method has emerged as the preferred choice, outperforming the PS-PWM method in terms of both efficiency improvement and total harmonic distortion (THD) reduction. The PLECS measurements have substantiated that the CH5MLI topology allows for reduced switching losses compared to the conventional CHBMLI topology. Specifically, the switches in the H-bridge section of the CH5MLI contribute to lower power losses than their counterparts in the CHBMLI.

This study's contributions lie in the enhanced understanding of the CH5MLI topology's dynamic behavior, the efficacy of employed modulation strategies, and its robust efficiency performance under varying operational conditions.

CRediT authorship contribution statement

Hakki Mollahasanoglu: Writing – original draft, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Merve Mollahasanoglu:** Writing – original draft, Methodology, Investigation, Conceptualization. **Emre Ozkop:** Writing – review and editing, Visualization, Supervision, Methodology, Investigation, Formal analysis, Data

curation, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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